CASE STUDY

Verification of MIPI MPHY Analog IP Leveraging Verilog-AMS

THE CLIENT

The client is a leader in smartphone market, home appliances, home entertainment and consumer electronics.

BUSINESS NEED

The client wanted ALTEN Calsoft Labs to model a MIPI MPHY analog IP using Verilog-AMS with wreal and verify the model using a UVM-MS based testbench environment.The verification of the MPHY model was to be performed as follows.

- Verification of the standalone analog MPHY model
- Verification of the analog MPHY model with the client digital MPHY IP to verify the integration and the functions of the combined analog and digital block

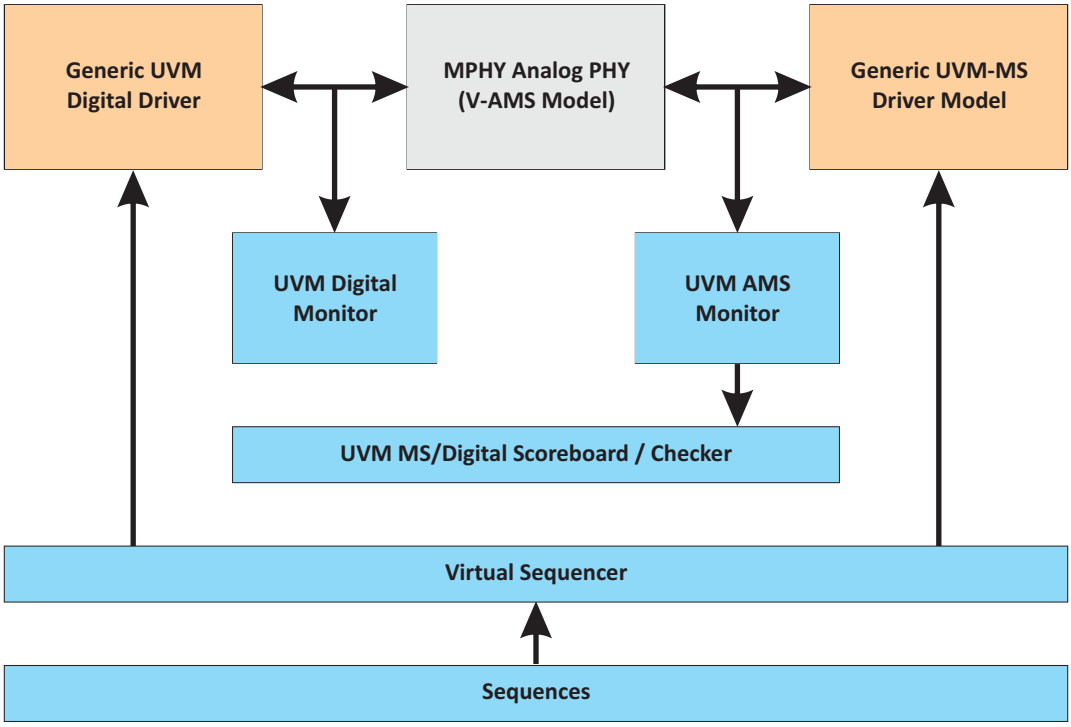
TECHNOLOGY USED

- **Language:** Verilog-AMS
- **Protocols:** UniPro, LLI, DigRFv4
- **Symbol Coding:** 8b10b

SOLUTION DELIVERED

ALTEN Calsoft Labs did the following to deliver the cost-effective yet efficient solution on time.

- Gathered design specification, schematics and implementation details for each sub-block of the analog MPHY IP design from the client
- Elicited scenario descriptions, test input vectors and output waveforms from a number of client spice simulations for verification purpose
- Ported the collected data to the UVM test bench and then compared the UVM results with the reference results
- Extracted features from the specifications and converted these into directed and constrained random test cases
- Executed the project using a phased delivery plan with a "blended" team split between onsite and offshore
- Performed the work in three phases with deliverables reviewed at the end of each phase
  - In the first phase, the spice simulations were analysed and a feature extraction was performed to generate a functional coverage proposal. The phase-1 was signed-off by reviewing the feature extraction, functional coverage document, testbench architecture document, development of verification environment using UVM-MS, implementation of 50% Verilog-AMS MPHY IP model and bringing up test cases on the model.
  - For Phase-2 signoff, ALTEN Calsoft Labs' expert team completed implementing the fully-functional Verilog-AMS model and verification was completed with 70% functional coverage.
  - For Phase-3, the team achieved 100% functional and code coverage closure.
- Provided regular detailed functional coverage reports and results from checks between the Spice and behavioural model simulations



BUSINESS BENEFITS

- 100% functional coverage closure within three months
- Cost effective solution utilizing a blend of onsite and offshore resources
- Allowed to track milestone delivery for each phase and achieve signoff in a methodical manner
- Complementary detailed VIP user guide and test plan document

ABOUT ALTEN CALSOFT LABS

ALTEN Calsoft Labs is a next gen digital transformation, enterprise IT and product engineering services provider. The company enables clients innovate, integrate, and transform their business by leveraging disruptive technologies like mobility, big data, analytics, cloud, IoT and software-defined networking (SDN/NFV). ALTEN Calsoft Labs provides concept to market offerings for industry verticals like education, healthcare, networking & telecom, hi- tech, ISV and retail. Headquartered in Bangalore, India, the company has offices in US, Europe and Singapore. ALTEN Calsoft Labs is a part of ALTEN group, a leader in technology consulting and engineering services.

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