Overview

Today’s ASIC/SoC designers are faced with the challenge of managing increasing complexity in functionality, integration of multiple processor cores & hardware acceleration engines, increasing chip size, decreasing time-to-market and decreasing power consumption. Design and Verification of complex ASICs/SoCs therefore requires serious domain knowledge to understand the functional requirements, develop block & system-level models, and methodology-driven test bench creation to ensure excellent test coverage keeping time-to-market constraints in mind.

ALTEN Calsoft Labs offers state-of-the-art VLSI design and verification services to semiconductor vendors and custom ASIC designers in Networking, Wireless, Mobile Multimedia and Consumer Electronics markets. At ALTEN Calsoft Labs, we specialize in front-end design and verification for complex multi-million gate ASICs/SOCs with multiple RISC/DSP cores and hardware accelerators.

Our Services

Systems architecture & RTL design

ALTEN Calsoft Labs works with Tier-1 silicon vendors and fabless semiconductor companies from Spec-to-Netlist. ALTEN Calsoft Labs is one of the few companies that help customers in system-level model and design partitioning using proven methodologies, ESL tools and rich domain expertise in networking, multimedia and wireless. Our services include:

- **System architecture & Partitioning**
  - Block / System-level modeling
  - Transaction Level modeling (TLM)
  - Architecture validation

- **Front-end Design**
  - RTL design
  - IP integration
  - Logic synthesis & Timing analysis

ALTEN Calsoft Labs works with its qualified partners specializing in Physical Design & Verification to offer end-to-end RTL-to-GDS2 capabilities to customers looking for one-stop silicon design house.

Verification & Validation

Over the last few years ALTEN Calsoft Labs has emerged as a leading ASIC/SOC design verification house with capabilities in IP verification, Block/Sub-system level verification and System-level verification & validation of complex SOCs. We have successfully verified systems with multiple clocks, power domains and speeds up to 1.2 GHz. We focus on the latest verification methodologies – eRM, OVM, VMM and UVM with special emphasis on re-usability of test benches at Block, Sub-system and System level, thereby helping our customers save time in complex ASIC/SoC verification process.
Our services include:

**ASIC/SOC Verification**
- Test bench design / development
- Verification IP development
- Functional Verification at Block, Sub-system or System level
- Model-based Verification
- Hardware-Software Co-Verification
- Coverage-driven Verification
- Assertion-based Verification
- Constrained-Random Verification
- Low Power (CPF / UPF) Verification
- Test bench migration to e/Vera/SystemVerilog

**System Validation**
- ASIC prototyping on FPGA
- Functional Validation
- Performance Testing
- Conformance & Interoperability Testing
- Load and Stress Testing
- Board Bring up
- Software Integration and Testing

**Key Differentiators**

- **Methodology oriented**: ALTEN Calsoft Labs lays special emphasis on re-usability of test benches at Block, Sub-system and System level in SOC verification engagements. Our focus on the latest verification methodologies – eRM, OVM, VMM and UVM, ensure that we put together high quality teams that mitigate project risks for customers.

- **Systems knowledge**: ALTEN Calsoft Labs leverages its domain knowledge in having worked on 1000+ products in networking, media, consumer electronics and industrial control markets to offer skilled resources that understand the DOMAIN and latest TOOLS to deliver high productivity and better functional coverage in SOC verification projects.

- **Low-Power verification**: ALTEN Calsoft Labs has a core team that specializes in LP test case development and debugging using CPF/UPF tools. Good understanding of low power concepts, power domains and clock gating techniques allows our team to verify power domains individually and cumulatively based on the application/product use cases.